What is claimed is:

1. A synchronous transfer mode (STM)-256 adder/dropper comprising:

first through fourth STM-64 adders/droppers, which multiplex STM signals at a low speed between an STM-256 framer and an optical transceiver, add and drop the STM signals, and provide synchronized data to the STM-256 framer and the optical transceiver; and

a switch unit, which switches data input/output of the STM-64 adders/droppers.

2. The STM-256 adder/dropper of claim 1, further comprising:

a clock generator, which generates an internal resonance clock signal; and

a multiplexer, which selects one from a clock signal generated in the clock generator and an externally-input clock signal and transmits the selected clock signal to the first through fourth STM-64 adders/droppers and the switch unit.

3. The STM-256 adder/dropper of claim 1, wherein each of the STM-64 adders/droppers comprises:

an STM-64 dropper, which analyzes an overhead of a frame of the STM signals and outputs the STM signals to one of a signal path of the STM-256 framer and an input path of the switch unit according to the analyzed result; and

an STM-64 adder, which adds a frame transmitted from the switch unit to flow of the frame from the STM-256 framer to lower sub-networks.

4. The STM-256 adder/dropper of claim 1, wherein the overhead of the frame of the STM signals comprises:

a first control byte, which indicates adding or dropping of a data frame;

a second control byte that represents a dispatch address of the added or dropped data frame;

a third control byte that represents a destination address of the added or dropped data frame; and

a fourth control byte that represents whether a payload of the data frame is vacant.

5. The STM-256 adder/dropper of claim 3, wherein, if it is determined that the payload of the frame is vacant, the STM-64 adder adds a frame transmitted from the switch unit to the vacant region.

6. The STM-256 adder/dropper of claim 3, further comprising a memory, which is connected between each of the STM-64 adders and the switch unit and stores the frame transmitted from the switch unit when the overhead of the frame is analyzed.

7. The STM-256 adder/dropper of claim 3, further comprising first through fourth input buffers, which are connected to an input terminal of each of the STM-64 droppers, and wherein the input buffers use a clock signal transmitted from the optical transceiver as an input side clock signal and use an internal clock signal of the STM-256 adder/dropper as an output side clock signal.

8. The STM-256 adder/dropper of claim 3, further comprising first through fourth output buffers, which are connected to an output terminal of each of the STM-64 droppers, and wherein the output buffers use an internal clock signal of the STM-256 adder/dropper as an input side clock signal and use a clock signal transmitted from the STM-256 framer as an output side clock signal.

9. The STM-256 adder/dropper of claim 3, further comprising fifth through eighth input buffers, which are connected to an input terminal of each of the STM-64 adders, and wherein the input buffers use a clock signal transmitted from the STM-256 framer as an input side clock signal and use an internal clock signal of the STM-256 adder/dropper as an output side clock signal.

10. The STM-256 adder/dropper of claim 3, further comprising fifth through eighth output buffers, which are connected to an output terminal of each of the STM-64 adders, and wherein the output buffers use an internal clock signal of the STM-256 adder/dropper as an input side clock signal and use a clock signal transmitted the optical transceiver as an output side clock signal.

11. The STM-256 adder/dropper of claim 1, wherein the switch unit comprises:

a switch, which connects the frame transmitted from each of the STM-64 droppers to an arbitrary STM-64 adder corresponding to a destination;

an interpreter, which interprets the overhead of the frame transmitted from each of the STM-64 droppers and obtains information on the destination; and

a switch controller, which controls a path of the switch in response to the information obtained by the interpreter.

12. The STM-256 adder/dropper of claim 11, wherein the switch unit further comprises a data memory, which is connected to the interpreter and the switch and prevents the frame from being simultaneously output to the same destination port.

13. The STM-256 adder/dropper of claim 11, wherein the switch unit further comprises an output buffer, which temporarily stores the frame output from the switch.

14. The STM-256 adder/dropper of claim 11, wherein the switch is a 4 x 4 electrical switch.